Attorney Docket: RPS920030106US1/2873P

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Jinny Nguyen

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In Re Application of:	Date: September 19, 2005
Patrick H. BUFFET et al.	Confirmation No.: 6420
Serial No.: 10/644,372	Group Art Unit: 2891
Filed: August 20, 2003	Examiner: Thai, Luan C.

For: METHODS TO REDUCE SIGNAL CROSS-TALK

APPEAL BRIEF

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I. REAL PARTY IN INTEREST

Appellant respectfully submits that International Business Machines Corporation is the real party in interest.

II. RELATED APPEALS AND INTERFERENCES

Appellant states that no such proceeding exists.

III. STATUS OF CLAIMS

Claims 1, 5-7, 15, 17-18, and 22-23 are pending and stand rejected. Accordingly, claims 1, 5-7, 15, 17-18, and 22-23 are on appeal and all applied rejections concerning those claims are herein being appealed.

IV. STATUS OF AMENDMENT

On January 12, 2005, Appellant filed an Amendment in response to an Office Action dated November 11, 2004. In this Amendment, claims 1, 5-6, 15, 17-18, and 22 were amended, and claims 2-4, 8-14, 16, and 19-21 were canceled Appellant notes that Examiner rejected claim 24 in this Office Action, however, no claim 24 as filed.

On June 30, 2005, Appellant filed a response to a Final Office Action dated April 4, 2005. Appellant submitted remarks/arguments to the rejection of all pending claims. No claims were amended, added, or canceled.

In an Advisory Action dated July 19, 2005, the Examiner states that this response will not be entered for purposes of appeal because they do not place the application in better form for appeal by materially reducing or simplifying the issues for appeal, for the reasons of record noted in the final rejection dated April 4, 2005.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The present invention provides, in independent claims 1 and 15, a multi-layer semiconductor chip package and a connector capable of being coupled to a semiconductor chip package, comprising: a plurality of pairs of conductors for carrying a plurality of signals in a layer of a carrier of the package, wherein each pair of conductors in the layer is positioned so that adjacent pairs of conductors affect each other evenly, wherein cross-talk between the adjacent pairs of conductors is substantially minimized without increasing a size of the package.

The present invention further provides, in independent claim 18, a method for providing a semiconductor chip package, comprising the step of providing a plurality of pairs of conductors for carrying a plurality of signals in a layer of a carrier of the package, wherein each pair of conductors in the layer is positioned so that adjacent pairs of conductors affect each other evenly, wherein cross-talk between the adjacent pairs of conductors is substantially minimized without increasing a size of the package.

Figures 5A and 5B illustrates an embodiment of the claimed multi-layer semiconductor chip package. As illustrated in Figure 5A, the pair of RX conductors 502 is positioned so that the TX conductor T3 evenly affects RX conductors R5 and R7. The pair of TX conductors 503 is also positioned so that the TX conductor T2 evenly affects TX conductors T1 and T3. Similarly, the RX conductor R6 is evenly affected by TX conductors T2 and T4, and the RX conductor R7 is evenly affected by RX conductors R6 and R8. Here, the pairs of conductors are positioned orthogonally to each other. With this conductor configuration, cross-talk between adjacent conductors is substantially minimized without increasing the size of the package. (Specification p. 7, line17 through p. 8, line 5)

As illustrated in Figure 5B, the pair of RX conductors 505 are positioned so that the RX conductor R3 is evenly affected by RX conductors R5 and R7. A pair of TX conductors 507 are also positioned so that the TX conductor T2 evenly affects RX conductors R1 and R3. Similarly, the TX conductor T6 evenly affects TX conductors T2 and T4, and the RX conductor R7 is evenly affected by TX conductors T6 and T8. With this conductor configuration, cross-talk between adjacent conductors is also substantially minimized without increasing the size of the package. In short, to cancel out the cross-talks between adjacent conductors, each aggressor signal is kept at an equal distance to a victim signal. (Specification p. 8, lines 6-16)

The present invention thus reduces the cross-talk without compromising the density of the interconnections in the package or resulting in an increase in the size of the package. As illustrated in Figures 7 and 8, the present invention is also applicable to cross-talk between conductors in connectors.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Appellant respectfully seeks review of the following rejections:

1. Claims 1, 5-7, 15, 17-18, and 22-23 are rejected under 35 U.S.C. 102(e) as being anticipated by Arima et al (6,479,758).

2. Claims 1, 5, 15, 18, and 22 are rejected under 35 U.S.C. 102(e) as being anticipated by Stearns et al (6,215,184)

3. Claims 1, 7, 15, 18, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin (6,657,310).

VII. ARGUMENTS

A. Summary of the Applied Rejections

In the Final Office Action, the Examiner rejects claims 1, 5-7, 15, 17-18 and 22-23 under 35 U.S.C. 102(e) as being anticipated by Arima et al (6,479,758). The Examiner states:

> ...Regarding claims 1, 5-7, 15 and 17, Arima et al (see specifically figures 1-2 and 17A attached) disclose a multi-layer semiconductor chip package, comprising: a plurality of pair of conductors (X) for carrying a plurality of signals in a layer of a carrier (205, see figure 17A) having a similar terminals arrangement as shown in figure 1 (Col. 8, lines 8-50); wherein the adjacent pairs of conductors (X) in the layer are positioned orthogonally and equidistantly to each other so that adjacent pairs of conductors (X) affect each other evenly, and wherein the layer is near an interface between the carrier and a chip (see figure 17A). By forming the package as described above, even if signal wiring are closely arranged, it is possible to prevent cross-talk from occurring and it is possible to prevent the size from (see the Abstract and Col. 2, lines 1-4, Col. 6, lines 16-25, Col. 8, lines 1-7, Col. 9, lines 41-44, Col. 10, lines 5-9, and Col. 12, lines 42-45).
>
> Regarding claims 18 and 22-23, it should be noted that although claims 18 and 22-23 are "method claims", the method steps consist of the broad steps of "providing..., positioning... etc."; therefore, these steps would be inherently satisfied by the apparatus of the reference as modified.

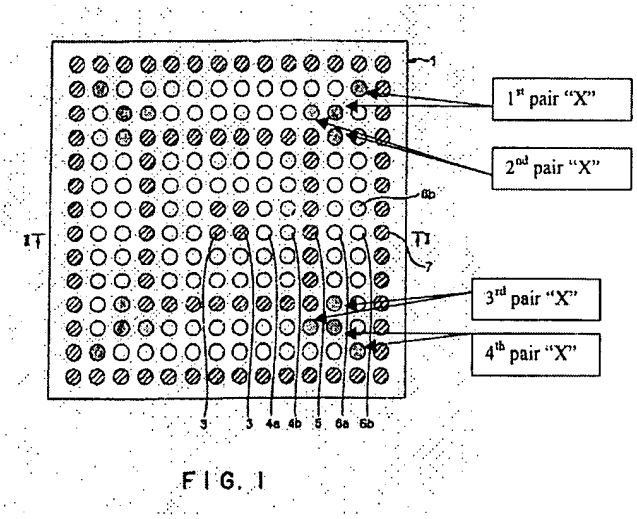

FIG. 1

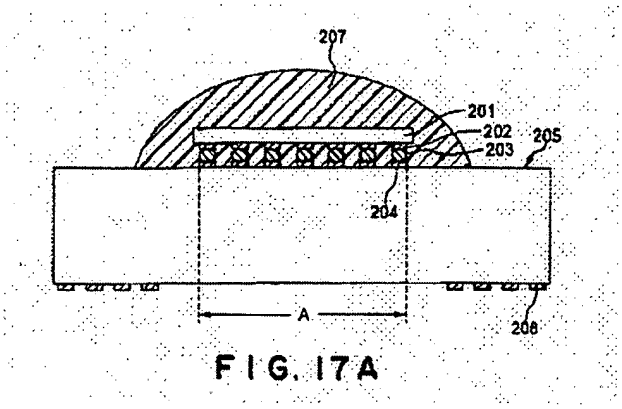

FIG. 17A

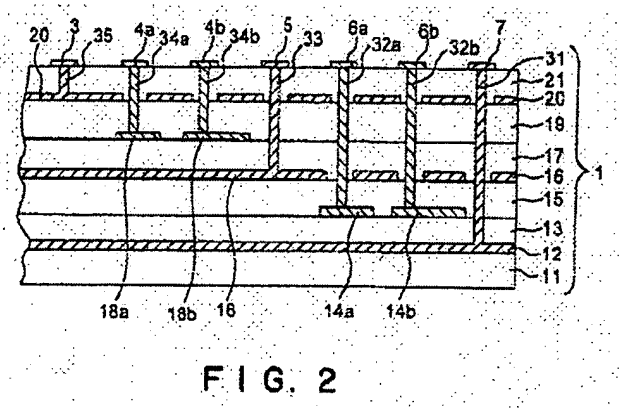

FIG. 2

The Examiner further rejects claims 1, 5, 15, 18 and 22 under 35 U.S.C. 102(e) as being anticipated by Stearns et al (6,215,184). The Examiner states:

> ...Regarding claims 1, 5, and 15, Stearns et al (see specifically figure 4 attached and Col. 2-3) disclose a multi-layer semiconductor chip package, comprising: a plurality of pairs of conductors (X) for carrying a plurality of signals in a layer of a carrier (1) of the package, wherein the adjacent pairs of conductors (X) are positioned orthogonally to each other and affect each other evenly. Stearns et al. teach that the advantages of the layout described above are: improved electrical performance, suitability for high frequency applications and flexibility to use nearly all signal traces as differential pairs or signal ended lines and reduced cross talk (see Col. 2, lines 56+).
>
> Regarding claims 18 and 22, it should be noted that although claims 18 and 22 are "method claims", the method steps consist of the broad steps of "providing..., positioning... etc."; therefore, these steps would be inherently satisfied by the apparatus of the reference as modified.

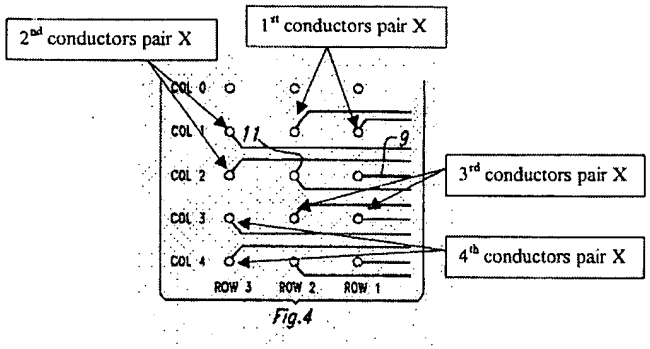

Fig.4

The Examiner further rejects claims 1, 7, 15, 18 and 23 under 35 U.S.C. 103(a) as being unpatentable over Lin (6,657,310). The Examiner states:

> Regarding claims 1, 7, and 15, Lin discloses (see specifically figures 10) a multi-layer semiconductor chip package, comprising: a plurality of pairs of conductors, wherein the first pair of conductors are the vertical wirings (131) connected to bumps (101-102), for carrying a first signal in a layer near an interface between the carrier (130) and a chip (100), and wherein the second pair of conductors are the vertical wirings 131 connected to bumps 103-104, for carrying a second signal adjacent to the first pair of conductors in the layer. Thus, all the claimed structure of the invention has been taught. Lin does not explicitly disclose cross-talk between the first and second pairs of conductors being substantially minimized.
>
> Since applicant's claimed structures in claims 1, 7, and 15 do not distinguish over the Lin reference, the claimed of "cross-talk being substantially minimized" could have been obvious to be included in Lin's structure.
>
> Regarding claim 18 and 23, it should be noted that although claims 18 and 23 are "method claims", the method steps consist of the broad steps of "providing..., positioning... etc."; therefore, these steps would be inherently satisfied by the apparatus of the reference as modified.

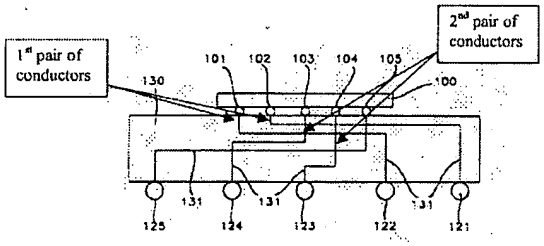

FIG. 10

B. The Cited Prior Art

Arima et al (6,479,758) discloses a wiring board having a plurality of wiring layers, a plurality of signal wiring terminals and a plurality of power supply terminals arranged on the principal plane of the wiring board, the signal wiring terminals or the power supply terminals being connected to any one of inner layers of the wiring layers, and signal writing terminals, which are connected to wirings formed on the same layer, among the plurality of signal writing terminals are arranged so that at least one side of the inside and outside of a region, in which the signal wiring terminals connected to the wirings formed on the same layer are formed, is surrounded by the power supply terminals. Thus, even if the signal wirings are closely arranged, it is possible to prevent crosstalk from occurring and it is possible to prevent the size from increasing. (Abstract)

Figures 1 and 2 of Arima illustrate a plan view and a sectional view, respectively, of a wiring board comprising an insulating layer 11 having a conductive layer 12; an insulator film 13 on insulating layer 11 with wiring patterns 14a and 14b formed on the principal plane; an insulating layer 15 on the insulting layer 13 with conductive layer 16; an insulating layer 17 on the insulating layer 15 with wiring patterns 18a and 18b;an insulating layer 19 on insulating layer 17 with a conductive layer 20; and an insulating board 21 on the insulting layer 19 with a plurality of terminals. The terminals are arranged in the form of a matrix as shown in Figure 1.

Figure 17A of Arima illustrates a modified example where the mounting surface for a semiconductor chip ahs the same terminal arrangement as that shown in Figure 1.

Stearns et al (6,215,184) discloses a method of laying out traces for connection of bond pads of a semiconductor chip to a printed wiring board or the like and the layout. (Abstract) The path traversed by each trace of each differential wiring pair is adjusted to have a pitch or distance

therebetween substantially equal to or less than a ball pitch to be parallel to each for the maximum possible distance, to each be as close as possible to the same length and to have the same cross-sectional geometry to the closest extent possible. (Col. 2, lines 1-26) Figure 4 of Stearns illustrates a preferred layout using three row so vias for connection to the chip and a pair of traces between each pair of columns of vias, according to the method disclosed.

Lin (6,657,310) discloses a method of closely interconnecting integrated circuits contained within a semiconductor wafer to electrical circuits surrounding the semiconductor wafer. Electrical interconnects are held to a minimum in length by making efficient use of polyamide or polymer as an inter-metal dielectric thus enabling the integration of very small integrated circuits within a larger circuit environment at a minimum cost in electrical circuit performance. (Abstract) Figure 10 of Lin illustrates the usage of common power, ground and signal pads for BGA devices using its disclosed invention. By using the BGA substrate 130 and the wiring 131 that is provided within the substrate, the BGA pads can be arranged in a different and arbitrary sequence that is required for further circuit design or packaging. (Col. 8, lines 15-28)

C. Claims 1, 5-7, 15, 17-18 and 22-23 are not anticipated by Arima et al. under 35 U.S.C. 102(e).

Appellant submits that Arima does not teach or suggest the present invention as recited in independent claims 1, 15, and 18. Appellant has reproduced the Fig. 1 of Arima with numerical references used by the Examiner as well as additional references corresponding to the Applicant's arguments as set forth below.

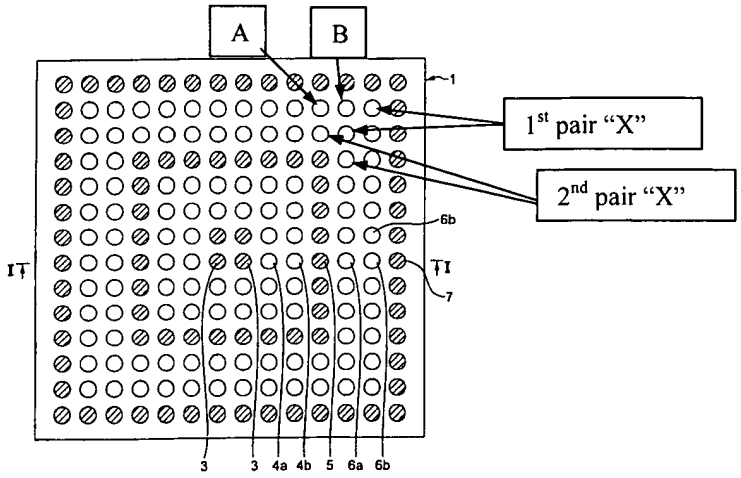

FIG. 1

In accordance with the present invention, a layer of a carrier or the chip package comprises a plurality of pairs of conductors, where each pair of conductors in the layer is positioned so that adjacent pairs of conductors affect each other evenly, where cross-talk between adjacent pairs of conductors is substantially minimized without increasing a size of the package.

The Examiner points to conductor pairs labeled "1st pair X" and "2nd pair X" in the Office Action in Fig. 1 of Arima as being positioned to be orthogonal and equidistant to each other. However, unlike the present invention, not *each* pair of conductors in the layer disclosed in Arima is so positioned. Rather, the positions of the conductors in Arima is more analogous to the prior art positioning set forth in Figures 2A and 2B of the specification, where some adjacent pairs affect each other unevenly.

For example, the conductors A and B in Fig. 1 of Arima (see above) makes up another pair of conductors. Although conductor B may affect the two conductors of the first pair evenly, conductor A does not since it is not equidistant from both conductors of the first pair. The same is true between conductors A and B and the second pair. Thus, in Arima not *each* pair of conductors in the layer as positioned so that adjacent pairs of conductors affect each other evenly,

as recited in the pending independent claims.

Thus, Arima does not teach or suggest the plurality of pairs of conductors where each pair of conductors in the layer is positioned so that adjacent pairs of conductors affect each other evenly, as recited in independent claims 1, 15, and 18.

In view of the foregoing, it is submitted that claims 1, 15, and 18 are allowable over Arima et al. Claims 5-7, 17, and 22-23 depend upon claims 1, 15, and 18, respectively, and are allowable because they are dependent upon allowable independent claims.

D. Claims 1, 5, 15, 18, and 22 are not anticipated by Stearns et al under 35 U.S.C. 102(e).

Appellant submits that Stearns et al does not teach or suggest the present invention as recited in independent claims 1, 15, and 18. Appellant has reproduced the Examiner's Fig. 4 of Sterns with additional numerical references corresponding to the Applicant's arguments as set forth below.

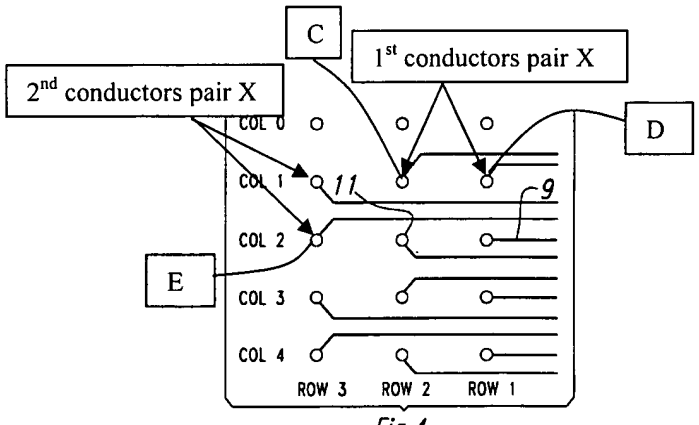

Fig.4

The Examiner points to conductor pairs labeled "1st conductors pair X" and "2nd conductors pair X" in the Office Action in Fig. 4 of Stearns as being orthogonal to each other.

However, unlike the present invention, not *each* pair of conductors in the layer disclosed in Stearns is so positioned. For example, the distance of conductor E of the 2nd conductors pair is from conductor C of the 1st conductors pair is not the same as its distance from the conductor D of the 1st conductors pair. The same is true for the distance of conductor F of the 2nd conductors pair from conductors C and D of the 1st conductors pair. Thus, the 1st and 2nd conductors pairs affect each other unevenly.

Thus, Stearns does not teach or suggest the plurality of pairs of conductors where each pair of conductors in the layer is positioned so that adjacent pairs of conductors affect each other evenly, as recited in independent claims 1, 15, and 18.

In view of the foregoing, it is submitted that claims 1, 15, and 18 are allowable over Stearns et al. Claims 5 and 22 depend from claims 1 and 18, respectively, and are allowable because they are dependent upon allowable base claims.

E. Claims 1, 7, 15, 18 and 23 are not unpatentable over Lin under 35 U.S.C. 103(a).

Appellant submits that Lin does not teach or suggest the present invention as recited in independent claims 1, 15, and 18. The Examiner points to conductor pairs labeled "1st pair of conductors" and"2nd pair conductors" in the Office Action in Fig. 10 of Lin as being orthogonal to each other. However, unlike the present invention, not *each* pair of conductors in the layer disclosed in Lin is so positioned. For example, the distance of conductor 103 of the 2nd pair from conductor 101 of the 1st pair is not the same as its distance from conductor 101 of the 1st pair. The same is true for the distance of conductor 104 of the 2nd conductors pair from conductors 101 and 102 of the 1st conductors pair. Thus, the 1st and 2nd pairs of conductors affect each other unevenly.

In view of the foregoing, it is submitted that claims 1, 15, and 18 are allowable over Lin. Claims 7 and 23 depend from claims 1 and 18, respectively, and are allowable because they are dependent upon allowable base claims.

F. Summary of Arguments

For the reasons set forth above, Appellant respectfully submits that the claims 1, 5-7, 15, 17-18, and 22-23 are allowable over the cited references. Appellant respectfully requests that the final rejection of these claims be reversed.

Note: For convenience of detachment without disturbing the integrity of the remainder of pages of this Appeal Brief, Appellants' APPENDICES A-C are attached on separate sheets following the signatory portion of this Appeal Brief.

Please charge any fee that may be necessary for the continued pendency of this application to Deposit Account No. 09-0460 (IBM Corporation).

Respectfully submitted,

SAWYER LAW GROUP LLP

September 19, 2005
Date

/Michele Liu/ Reg. No. 44,875
Michele Liu
Attorney for Appellant
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APPENDIX A

CLAIMS

1. A multi-layer semiconductor chip package, comprising:

a plurality of pairs of conductors for carrying a plurality of signals in a layer of a carrier of the package, wherein each pair of conductors in the layer is positioned so that adjacent pairs of conductors affect each other evenly,

wherein cross-talk between the adjacent pairs of conductors is substantially minimized without increasing a size of the package.

2. – 4. (canceled)

5. The package of claim 1, wherein the adjacent pairs of conductors are positioned orthogonally to each other.

6. The package of claim 1, wherein the adjacent pairs of conductors are positioned to be equidistant to each other.

7. The package of claim 1, wherein the layer is near an interface between the carrier and a chip.

8. – 14. (canceled)

15. A connector capable of being coupled to a semiconductor chip package, comprising:

a plurality of pairs of conductors for carrying a plurality of signals in a layer of a carrier of the package, wherein each pair of conductors in the layer is positioned so that adjacent pairs of conductors affect each other evenly,

wherein cross-talk between the adjacent pairs of conductors is substantially minimized without increasing a size of the package.

16. (canceled)

17. The connector of claim 15, wherein the adjacent pairs of conductors are positioned to be equidistant to each other.

18. A method for providing a semiconductor chip package, comprising the steps of:

(a) providing a plurality of pairs of conductors for carrying a plurality of signals in a layer of a carrier of the package, wherein each pair of conductors in the layer is positioned so that adjacent pairs of conductors affect each other evenly,

wherein cross-talk between the adjacent pairs of conductors is substantially minimized without increasing a size of the package.

19. – 21. (canceled)

22. The method of claim 18, wherein the adjacent pairs of conductors are positioned

to be equidistant to each other.

23. The method of claim 18, wherein the layer is near an interface between the carrier and a chip.

APPENDIX B

EVIDENCE

(NONE)

APPENDIX C

RELATED PROCEEDINGS

(NONE)

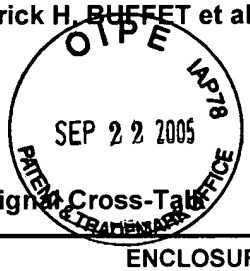
TRANSMITTAL FORM	Attorney Docket No. RPS920030106US1/2873P

In re the application of: **Patrick H. BUFFET et al.**

Serial No: **10/644,372**

Filed: **August 20, 2003**

For: **Method to Reduce Signal Cross-Talk**



Confirmation No: **6420**

Group Art Unit: **2891**

Examiner: **Thai, Luan C.**

ENCLOSURES *(check all that apply)*					
☐	Amendment/Reply	☐	Assignment and Recordation Cover Sheet	☐	After Allowance Communication to Group
	☐ After Final	☐	Part B-Issue Fee Transmittal	☐	Notice of Appeal
☐	Information disclosure statement	☐	Letter to Draftsman	■	Appeal Brief
	☐ Form 1449	☐	Drawings	☐	Status Letter
	☐ (X) Copies of References	☐	Petition	■	Postcard
☐	Extension of Time Request *	☐	Fee Address Indication Form	☐	Other Enclosure(s) (*please identify below):*
☐	Express Abandonment	☐	Terminal Disclaimer		
☐	Certified Copy of Priority Doc	☐	Power of Attorney and Revocation of Prior Powers		
☐	Response to Incomplete Appln	☐	Change of Correspondence Address		
☐	Response to Missing Parts	*Extension of Term: Pursuant to 37 CFR 1.136, Applicant petitions the Commissioner to extend the time for response for xxxxxx month(s), from to .			
	☐ Executed Declaration by Inventor(s)				

CLAIMS					
FOR	Claims Remaining After Amendment	Highest # of Claims Previously Paid For	Extra Claims	RATE	FEE
Total Claims	9	23	0	$ 50.00	$ 0.00
Independent Claims	3	5	0	$200.00	$ 0.00
				Total Fees	$ 0.00

METHOD OF PAYMENT	
☐	Check no. _____ in the amount of $ _____ is enclosed for payment of fees.
■	Charge **$500.00** to Deposit Account No. 50-0563 (IBM Corporation) for payment of fees.
■	Charge any additional fees or credit any overpayment to Deposit Account No. 50-0563 (IBM Corporation).

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT	
Attorney Name	Michele Liu, Reg. No. 44,875
Signature	*/Michele Liu/* Reg. No. 44,875
Date	September 19, 2005

CERTIFICATE OF MAILING

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